AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-42. (canceled)

43. (currently amended) A semiconductor device comprising:

an interconnection board having first and second surfaces, said interconnection board having a multilevel insulating resin layer and a multilayer wiring layer therein;

at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane;

at least a semiconductor chip mounted on said first surface of said interconnection board;

a buffer layer having a first surface contacting said second surface of said interconnection board;

a supporting plate spaced from a second surface of said buffer layer and defining a gap between said second surface of said buffer layer and said supporting plate, said supporting plate having plural holes therein;

at least one external electrode in one of said holes in said supporting plate and connected to said at least one external electrode pad through said buffer layer, said at least one external electrode having a diameter smaller than said one of said holes so as to define a space between said at least one electrode and an internal periphery of said one of said holes at a surface of said supporting plate opposite said buffer layer; and

a sealing resin in said gap and in said space surrounding and supporting said at least one external electrode.

44. (canceled)

45. (previously presented) The semiconductor device as claimed in claim 43, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.

46. (original) The semiconductor device as claimed in claim 45, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

47. (original) The semiconductor device as claimed in claim 46, further comprising at least a heat spreader provided on said at least semiconductor chip.

48. (original) The semiconductor device as claimed in claim 45, wherein further comprising an under-fill resin material

provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

49. (previously presented) The semiconductor device as claimed in claim 48, further comprising:

a stiffener spaced from at least one peripheral edge of said semiconductor chip; and

a heat spreader contacting said semiconductor chip and said stiffener.

50. (previously presented) The semiconductor device as claimed in claim 43, wherein said buffer layer comprises plural generally column shaped electrically conductive layers that connect said at least one external electrode to said at least one external electrode pad; and a supporting sealing resin material surrounding said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is in tight contact with said plural generally column shaped electrically conductive layers.

51. (previously presented) The semiconductor device as claimed in claim 50, wherein said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said at least one external electrode.

52. (original) The semiconductor device as claimed in claim 50, wherein said plural generally column shaped electrically conductive layers are made of a metal.

53. (original) The semiconductor device as claimed in claim 50, wherein said supporting sealing resin material is made of an organic insulative material.

54. (original) The semiconductor device as claimed in claim 43, wherein said external electrode comprises a solder ball.

55-85. (canceled)

86. (previously presented) A semiconductor device comprising:

a multilayer interconnection board having first and second surfaces, said first surface being opposite and spaced from said second surface;

an external electrode pad formed in a side of said second surface;

a semiconductor chip mounted in a side of said first surface;

a metallic post protruding from said external electrode pad;

a metallic frame formed in said side of said second surface to surround said metallic post, a gap being thereby formed between said metallic post and said metallic frame; and

a resin layer filling said gap.

87. (previously presented) The semiconductor device as claimed in claim 86, wherein said external electrode pad has an

exposed surface forming a substantially flat plane with said second surface.

88. (previously presented) The semiconductor device as claimed in claim 86, wherein a height of said metallic post from said second surface is substantially equal to a height of said metallic frame from said second surface.

89. (previously presented) The semiconductor device as claimed in claim 86, further comprising:

a solder ball connected to said metallic post;

a support plate provided on a surface of said resin layer and having a hole, in which said solder ball is inserted;

an inter-space being thereby formed between said solder ball and said hole; and

a resin material filling said inter-space.